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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,081	10/10/2003	Young-Hee Jung	053933-5055	9496
9629	7590	09/22/2004	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004			CLARK, SHEILA V	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/682,081

Applicant(s)

JUNG, YOUNG-HEE

Examiner

S. V. Clark

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10-10-2003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

Art Unit: 2815

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki.

Suzuki shows in figure 5A a die 14 having a circuit pattern formed thereon connected to solder balls 15. A printed circuit board 16 is shown for mounting said die and since the a one die is shown formed on what appears to be less than half of the board it is deemed that said board has an area at least %100 as large as the area of the die. Heat sink 19 is shown mounted on the die and an encapsulant 17 ( i.e. epoxy) is filled between the printed circuit board and the heat sink and die and printed circuit board. Solder balls 15 are shown formed at the bottom surface of the die and connected to said board.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al.

Wang et al shows in figure 3 a die 22 having a circuit pattern formed thereon connected to solder balls 26a. A printed circuit board 20 is shown for mounting said die and since the a one die is shown formed on what appears to be less than half of the board it is deemed that said board has an area at least %100 as large as the area of the die. Heat sink 32 is shown mounted on the die and an encapsulant 30 is filled between

Art Unit: 2815

the printed circuit board and the heat sink. Epoxy 24 is shown filled between the die and printed circuit board. Solder balls 15 are shown formed at the bottom surface of the die and connected to said board. Encapsulant 30 may be formed of epoxy as described in col. 1, line 63 in the contents of 5,285,352 incorporated by reference.


The die is attached to said board by an epoxy adhesive 24.

Figure 4 shows die connection with the use of wire bonding pads 26b and figure 3 shows use of solder balls 26a. Solder balls 28 are also shown formed on the bottom of board 20 for mounting to another board.

Claims 1-7 are rejected.

Borrow, Chia et al, Kim et al, Ando et al and Takubo are all cited to show chips, having heat sinks formed on a top surface and printed circuit boards formed on a bottom surface.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.

  
S. V. Clark  
Primary Examiner  
Art Unit 2815

September 18, 2004